RF mixers using standard digital CMOS 0.35µm process

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***Abstract* — The performance of doubly-balanced active and resistive RF CMOS mixers is presented following measurements at 1.8-GHz RF frequency. The active mixer has demonstrated 10.4-dB gain, 7-dB SSB NF, –6dBm IIP3 and consumes 9.7mA under 3V. The passive mixer has demonstrated 7.5-dB loss, 10-dB SSB NF and +16-dBm of input IP3.**

I. Introduction

The RF component market has grown very rapidly over the past ten years with the explosion of the cellular Telephone market, the emergence of high data rate communications, the optical infrastructures and the automotive market. To support such a growth, GaAs, that used to be the substrate of choice for RF functions, has been challenged by Bipolar and BiCMOS processes (including SiGe bipolar devices). But none of these processes has the cost structure of CMOS. That is why CMOS RF has naturally become the target of many RF designers. It was demonstrated [1] that to be capable of low production prices, standard digital CMOS process has to be used. CMOS has the advantage over the other technologies to offer a high production capacity. With reference to Fig. 1 it can be seen that it is profitable to share the market with a high production volume partner such as DRAMs to reach the lowest wafer cost of the CMOS foundry.

We have decided to create some of the key RF functions in standard CMOS for the purpose of later integration into large volume products. This presentation targets the mixer structures.

II. Technology

Both mixers have been fabricated using the ATMEL's standard digital 0.35-µm CMOS three-metal layer planar process. The epitaxy layer (slightly doped) is grown on an 8-in highly doped (with Bore), low resistive, silicon wafer (15mΩ.cm). A thick oxide layer (LOCOS) is used as isolation. This also allows a better control for the high-energy implantation of the retrograde wells.

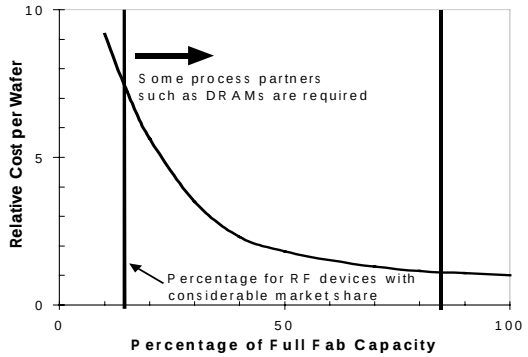

Fig. 1. Plot of the relative production cost versus the percentage of full CMOS foundry capacity.

The gate of NMOS and PMOS transistors is made of an N-doped polysilicon. The result is that the threshold voltages of the NMOS and the PMOS are not symmetric. The oxide planarization is obtained by CMP process. The metal used for the three metal interconnect layers is aluminum.

RF transistors have been designed in order to improve their frequency and noise performance. Multi-finger transistor structures have been investigated by varying the number of fingers (n) and the unity gate width (W_u). The resulting noise performance is directly concerned since the total gate resistance (R_g) is divided by a factor of n^2. The maximum oscillation frequency (f_{max}), depending for its part on W_u, has been maximized for a W_u of 10 microns.

III. Active Mixer

The differential cell is the core of our active mixer: it is an RF amplification stage with an LO switching quad stacked on.

Since the beginning of the design, the mixer has been devised to have 10 dB of RF-to-IF conversion gain (CG). That condition was difficult to reach using resistive loads. Therefore, as shown in Fig. 2, we used active loads to meet the specification and, as a consequence, a common mode feedback (CMFB).

We optimized the drain-to-source voltage (V_{ds}) and the overdrive voltage (V_{gs}–V_{Th}) of the RF and LO stages in terms of single-sideband noise figure (SSB NF) [2] and linearity (IIP3). Internal voltage for the CMFB and a self biased micro-current reference, with relative start-up voltage (ON), were integrated.

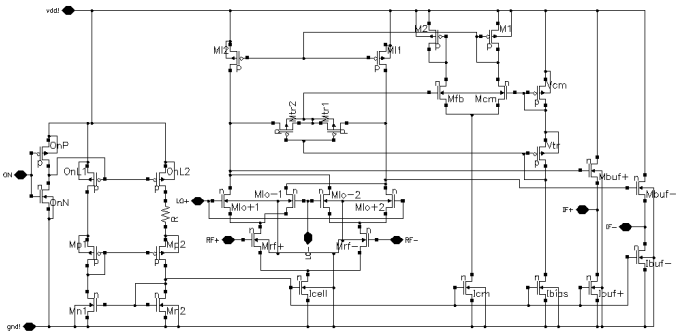

Fig. 2. The active mixer schematic.

A careful layout has been the next step of the design, where a guard ring of p+ connected to ground was used to ensure a stable substrate and to increase the isolation between the different functions. Besides, all the signal paths were ground-surrounded and the lead frame of the package was connected to ground by a special bonding between the frame itself and the die.

For the measurements we designed an FR4 multi-layer board (PCB). On the PCB were implemented 1.8-GHz 50Ω lines, SMD (0603) placements and 50Ω SMA connectors. Single-ended S-parameter measurements were first carried out onto a specific board location. An on-board TRL calibration kit (thru, open, λ/4 line), which takes account of the length of the access lines to the chip, was used to calibrate the vectorial network analyzer (VNA). The reference planes of the VNA are then located at the extremities of the package leads. The RF and IF ports were matched to 50 Ω respectively between the chip and the RF and IF baluns (balanced-to-unbalanced transformers). The access insertion loss from both sides of the chip (RF and IF) were then known and removed from the rough data. The measurements of the RF-to-IF conversion gain, the three port-to-port isolations, the linearity and the noise figure were done with a spectrum analyzer. Concerning the SSB noise figure measurement, we have used a 15-dB ENR noise source, a 25-dB gain 1.2-dB NF low noise amplifier to enhance the measurement dynamic and a Faraday cage in order to limit the surrounding radiation. Bandpass filters were used at the RF and the LO ports to be in accordance with the single-sideband noise figure definition.

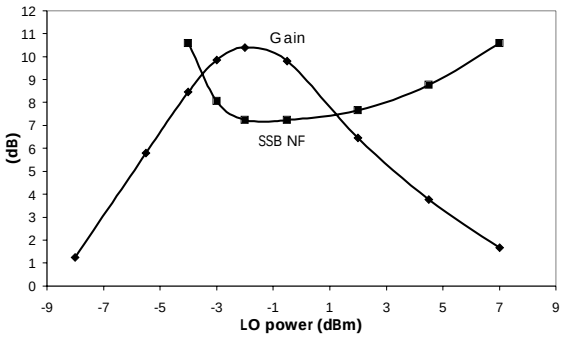

Fig. 3. RF-to-IF conversion gain and single-sideband noise figure of the active mixer.

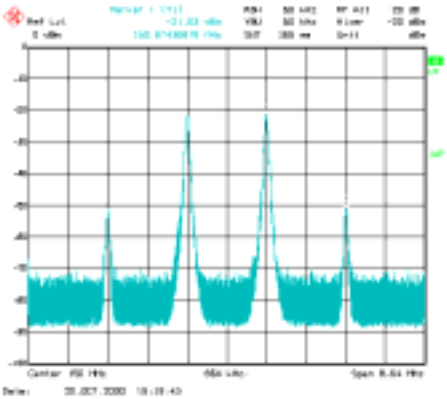

Fig. 4. IF intermodulation spectrum of the active passive.

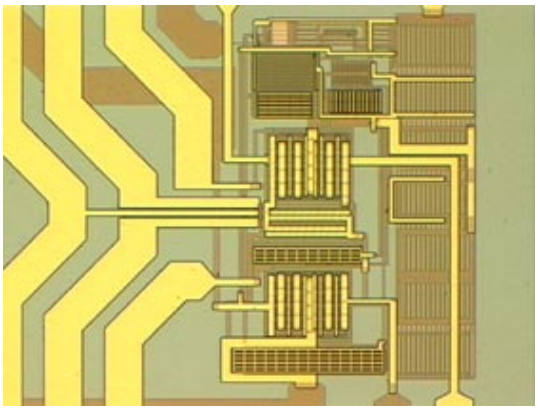

Fig. 5. Microphotograph of the active mixer chip.

The performance is summarized in Table 1. The current consumption is 9.7 mA: 5.2 mA in the mixing core, 1.4 mA in the CMFB, 2.6 mA in the output buffers. The mixer shows an RF-to-IF conversion gain of 10.4 dB (see Fig. 3), an SSB NF of 7.2dB, an IIP3 of –6dBm (see Fig. 4) and an input power at 1-dB compression of –19 dBm.

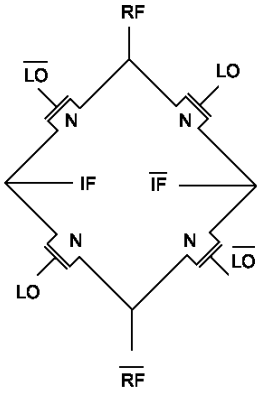

Fig. 6. The passive mixer schematic.

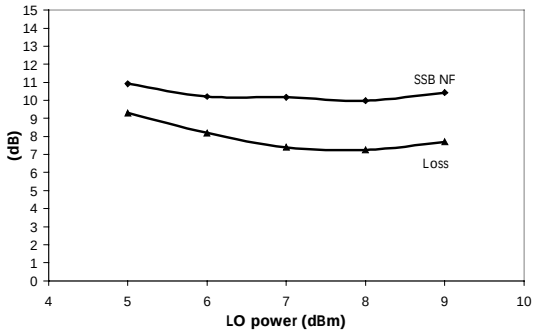

Fig. 7. RF-to-IF conversion gain and single-sideband noise figure of the passive mixer.

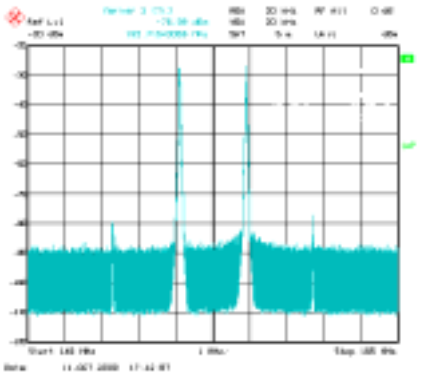

Fig. 8. IF intermodulation spectrum of the passive active.

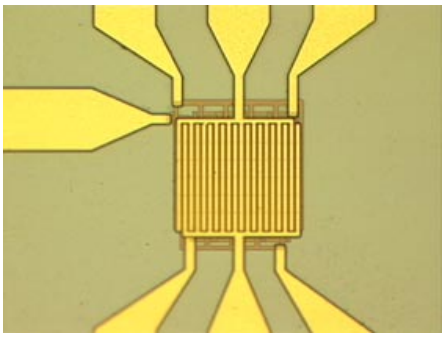

Fig. 9. Microphotograph of the passive mixer chip.

The optimum LO power level is –2 dBm and we find an isolation of 42 dB between RF-LO, 33 dB between RF-IF and 28 dB LO-IF. The layout is shown in Fig. 5, the mixer size is 0.29x0.42 mm².

IV. Passive Mixer

The doubly balanced passive CMOS mixer is comparable in terms of high linearity and low RF-to-IF conversion loss to the microwave diode mixer [3] and to the existing commercial products (built in GaAs or SOI).

When no dc drain-to-source voltage is applied, each NMOS transistor of Fig.6 operates in its linear region, as a switch. Each switch is driven between its "on" and "off" states by applying the LO signal to its gate. Besides, for optimum transfer, the LO signal should be applied along with dc gate bias around the NMOS threshold voltage (V_{th}).

In the "on" state, the transistor's drain-to-source impedance is equivalent to the low drain-to-source channel resistance, denoted R_{on}. In the "off" state, the drain-to-source impedance is equivalent to the drain-to-source capacitor, denoted C_{off}, assuming that this time the channel resistance is high.

The theoretical optimum conversion loss for an ideal balanced passive mixer is equal to $20\log(2/\pi)$=-3.9dB, assuming that the LO signal at the gate is a square waveform and the R_{on} resistance is zero [2].

The drain-to-source resistance (r_{ds}) depends directly on the transistor's geometry and in the linear region is given by:

$$r_{ds} = \frac{L}{\mu_n C_{ox} W [(V_{gs} - V_{th}) - V_{ds}]}, \qquad (1)$$

where L is the gate length, μ_n is the average electron mobility in the channel, C_{ox} is the gate oxide capacitor per unit area, and W is the gate width. Considering (1), R_{on} is minimized if the transistor is drawn with the minimum L (L_{min}) and a large W. The usual tendency is to use a large W but the gate-to-source and gate-to-drain capacitors proportionally increase with W. One can also note that the gate voltage swing (V_{gs}-V_{th}) contributes to decrease R_{on}. From that two-state representation, the frequency limitation of the passive mixer depends essentially on the $R_{on}xC_{off}$ product. That product is useful to assess the ability of the technology for such a passive mixer because it is independent from W but depends strongly on L_{min} and C_{ox}.

TABLE I
SUMMARY OF BOTH MIXER PERFORMANCES

	Passive Mixer	Active Mixer
Supply voltage (V)	-	3
DC Power consumption (mW)	0	29
RF-to-IF conversion gain (dB)	-7.5	10.4
SSB noise figure (dB)	10	7.2
P_{-1dB} (dBm)	+1	-19
Input IP3 (dBm)	+16	-6
LO power level (dBm)	+7	-2
LO frequency (GHz)	1.65	1.65
RF frequency (GHz)	1.8	1.8
LO-to-RF isolation (dB)	32	42
LO-to-IF isolation (dB)	27	28
RF-to-IF isolation (dB)	23	33

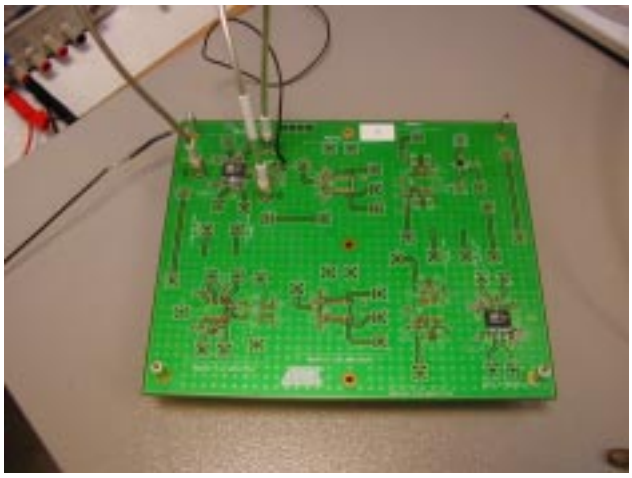

Fig. 10. Photo of the board.

The fully differential structure of the mixer provides virtual grounds at each port by the cancellation of the even order harmonics.

Because the on-state representation of a cold NMOS is essentially a small resistor, the passive mixer is able to reach high input IP3 but the disadvantage is large LO power requirement.

The implementation of the passive mixer is simple and presents no risk of instability. The measurements have been made following the same procedure as for the active mixer of section III. As shown in Fig. 7, the packaged passive mixer has demonstrated an RF-to-IF conversion gain of –7.5dB at a LO power of +7dBm. The associated SSB noise figure is 10dB. As expected, the input IP3, estimated from the spectrum of Fig.8, is high and is equal to +16dBm. As shown in Fig. 9, the layout of the passive mixer is compact and symmetrical. The circuit size is 0.1x0.1 mm².

V. CONCLUSION

This work has presented the performance of two encapsulated 1.8-GHz RF mixers (Fig. 10), one active and one passive, built in standard digital 0.35-µm CMOS process. The active mixer is a differential mixer using active loads, a common-mode feedback circuit, and output buffers. It has demonstrated 10.4-dB RF-to-IF conversion gain, 7.2-dB SSB noise figure and –6dBm IIP3. It consumes 29mW under 3V. For its part, the passive mixer has demonstrated –7.5dB loss, 10dB SSB NF and +16dBm IIP3 when consuming no DC power. The qualities of the passive mixer are its simplicity, its frequency stability and its high linearity; all these specifications making it a strong contender for multi-mode receivers. The linearity should be particularly appreciated since the limiting factor of receivers remains essentially in the linearity of the mixer.

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